REMARKS

Claims 1-70, 74-75, 77, and 82-88 are canceled; claims 91-100 are new; and claims 71-73, 76, 78-81, and 89-100 are pending in the application.

Claims 71 stands rejected for Walker et al. (U.S. 6,888,750) (hereinafter "Walker") in view of Yamazaki et al. (6,693,044) (hereinafter "Yamazaki-1") and Yamazaki et al. (6,759,677) (hereinafter "Yamazaki-2"). Claim 71 recites a computer system comprising:

> a signal source arranged to provide a data signal; and
>
> an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:
>
> a structure comprising silicon and germanium;
>
> a first transistor supported by the structure, the first transistor comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the structure, the first transistor being a PFET and the first source/drain regions accordingly being p-type doped regions; the first gate being substantially non-overlapping with respect to the first source/drain regions;
>
> an insulative material over at least a portion of the first transistor;

a first layer of semiconductive material over the insulative material;

a second layer of semiconductive material over the first layer, the second layer of semiconductive material physically contacting the first layer of semiconductive material, and the second layer of semiconductive material being compositionally different from the first layer of semiconductive material;

a second transistor over the insulative material, and supported by the first and second layers of semiconductive material, the second transistor comprising a second gate and a pair of second source/drain regions, the second transistor being an NFET and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the second layer of semiconductive material; the second gate being directly over the first gate; the second gate being substantially non-overlapping with respect to the second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.

The Examiner cites Figs. 12-14 and accompanying text of Walker as disclosing the signal source, inverter, and output recited by claim 71. The Examiner also cites Fig. 9 and accompanying text of Walker as disclosing a semiconductor structure of a first transistor and a second transistor of the inverter of Fig. 13 as recited by claim 71.

However, Fig. 9 and accompanying text is not related to the inverter of Walker's Fig. 13. In other words, Fig. 13 is not a schematic diagram of the semiconductor structure illustrated in Fig. 9. Walker provides, in Fig. 1 and accompanying text, a schematic overview of a nonvolatile memory array having three layers. The bottom layer is an SOI substrate 3. The middle layer is a driver circuit 2 formed over substrate 3. Finally, a top layer comprising nonvolatile memory devices is formed over the driver circuit layer 2. The driver circuit layer contains read/write circuitry used to write data to the top layer memory devices and to read data from the top layer memory devices. The top layer contains a regular array of nonvolatile memory devices used to store data supplied by the middle layer (the driver circuit layer).

Fig. 9 is a cross-sectional view of one embodiment of the top layer (the nonvolatile memory device layer). This embodiment comprises charge storage devices.

In contrast, Figs. 12-14 illustrate schematic diagrams of one embodiment of the middle layer of Fig. 1 (the driver circuit layer). Consequently, Fig. 9 does not illustrate the circuits schematically illustrated in Figs. 12-14.

Applicant notes that col. 17 lines 27-44 of Walker disclose that a charge storage device that functions as an antifuse when a conductive link has been formed through its charge storage region may be used within the middle layer (the driver circuit layer). The devices illustrated in Fig. 9 have charge storage layers used to store charge. These charge storage layers, however, are not antifuse devices because a conductive link is not formed through the charge storage layers. Thus, the devices illustrated in Fig. 9 are not the type of devices envisioned by Walker for use within the driver circuit layer.

Applicant notes that the above argument is substantially similar to the argument used in response to the Examiner's assertion (presented in the 20 Mar 07 Office Action) that Fig. 10A of Walker discloses the inverter of claim 71, which argument was favorably received by the Examiner as indicated in the 22 Aug 2007 Office Action.

Furthermore, the Examiner cites col. 14 line 68 through col. 15 line 2 of Walker as disclosing that the TFT EEPROMs depicted in Fig. 9 may be a mixture of PFETs and NFETs. While the cited section does disclose PMOS and NMOS transistors, these transistors are disclosed in relation to Fig. 11, which is described by Walker as being an embodiment of the driver circuit described above (the middle layer of Walker's nonvolatile memory array). Using PMOS and NMOS transistors in a driver circuit enables Walker to create logic for reading and writing information to a top layer of nonvolatile memory devices formed in a layer above the driver circuit layer.

The nonvolatile memory device layer comprises an array of nonvolatile memory devices accessed using bitlines and wordlines. Fig. 9 illustrates one embodiment of an array of nonvolatile memory devices. Walker does not disclose forming some of the memory devices of the memory device layer using PMOS and others of the memory devices using NMOS. Indeed, mixing PMOS and NMOS devices in the memory device layer would unnecessarily complicate the driver circuitry logic since control gate signals of one polarity would be used when reading or writing PMOS memory devices and control gate signals of another polarity would be used when reading or writing NMOS memory devices.

Accordingly, Walker's disclosure of PMOS and NMOS devices in a driver circuit layer such as that illustrated in Fig. 11 and described in col. 14 line 68 through col. 15 line 2 of Walker does not disclose the simultaneous use of PMOS and NMOS devices in a memory device layer such as the memory device layer illustrated in Fig. 9. Since the Examiner relies on such disclosure in the rejection of claim 71, Applicant respectfully asserts that such reliance is improper.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 71. Claims 72-73, 76, 78-81, and 89-96 depend from claim 71, and are therefore allowable for at least the reasons discussed above regarding claim 71.

New claims 92-95 and 97-99 are supported by, for example, Fig. 11 and paragraphs 91-100 of the specification.

New claims 96 and 100 are supported by, for example, paragraphs 59 and 96 of the original specification.

Claims 71-73, 76, 78-81, and 89-100 are allowable for at least the reasons discussed above. Applicant therefore respectfully requests that the Examiner's next action be a Notice of Allowance formally allowing all of the pending claims.

Respectfully submitted,

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